UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,078	10/10/2003	Gilbert Wolrich	10559/132002/P7871C/Intel	3059

20985 7590 11/04/2008

FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
NGUYEN, TOAN D	

ART UNIT	PAPER NUMBER
2416	

NOTIFICATION DATE	DELIVERY MODE
11/04/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/684,078	WOLRICH ET AL.	
	Examiner	Art Unit	
	TOAN D. NGUYEN	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *20-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :5/28/08,10/19/07,3/09/06,5/13/05,5/4/04,10/10/03.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528,163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-13, 15-19 and 24-25 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-27 of U.S. Patent No. 6,661,794. Although the conflicting claims 1-13, 15-19 and 24-25 are not identical, they are not patentably distinct from each other because the application's claims merely broaden the scope of the patented claims by not claiming some claim elements (i.e., the first control information designating a relative position of the first portion with respect to one or more other portions of the network packet, the one or more other portions including the second portion; the second control information designating a relative position of the second portion with respect to one or more other portions of the network packet, the one or more other portions including the first portion). The application's claims are nearly identical in every other respect to the patented claims. Therefore, the application's claims are simply broaden versions of the patented claims. It is Examiner's position that broaden the patented claims by not claiming some claim elements (i.e., the first control information designating a relative position of the first portion with respect to one or more other portions of the network packet, the one or more other portions including the second portion; the second control information designating a relative position of the second portion with respect to one or more other portions of the network packet, the one or more other portions including the first portion) of the patented claims would have been obvious to one of ordinary skill in

the art in view of the patented claims. It is important to note that the instant application is a combination of the application, which yielded the patent (USP 6,661,794) used herein as the basis for the obvious-type double-patenting rejection. The applicant is attempting to broaden the parent application's claims by deleting some of the claim elements in the continuation at issue here. If allowed, the application at bar would unjustly extend Applicant patent protection beyond the statutory period, at the same time, granting broader protection to the applicant.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 6-8 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Herring (US 6,606,326).

For claim 1, Herring discloses packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path, comprising:

a first port (figure 3, reference 310) to receive a network packet (col. 12, lines 11-12);

a second port (figure 3, reference 380) in communication with the first port (figure 3, reference 310), the second port to transmit the network packet after processing (col.

12, line 24);

circuitry (figure 1, reference 15) to associate first control information with a first portion of the network packet and to associate second control information with a second portion of the network packet (col. 9, lines 30-39);

circuitry (figure 1, reference 15) to process the first portion of the network packet and to process the second portion of the network packet at least partially in parallel with processing the first portion of the network packet (col. 9, lines 30-39); and

circuitry to enqueue (figure 3, reference 350) the first portion and the second portion for transmission to a second port in the same order in which the first portion and the second portion were received at the first port (col. 12, lines 35-38).

For claim 2, Herring discloses wherein the circuitry comprises:

one or more peripheral buses (figure 3, reference 315 and 370, col. 12, lines 35-42);

a memory system (figure 4, references 410, 420, 430 and 440, col. 15, lines 36-45);

a processor (figure 3, reference 340) coupled to the one or more peripheral buses and the memory system, the processor adapted to forward data from the first port to the second port (col. 14, lines 13-19); and

a bus interface to receive the first portion of the network packet and the second portion of the network packet from the first port and enqueueing the first portion and the second portion in the order in which they were received from the first port for

transmission to the second port, the first and second portions being processed at least partially in parallel (col. 16, lines 45-50).

For claim 6, Herring discloses wherein the one or more peripheral buses comprise at least one input-output bus, wherein the processor is adapted to interface over the input-output bus with at least one of a media access controller device and a high-speed device, the high-speed device comprising at least one of a gigabit Ethernet MAC and a dual gigabit MAC with two ports (figure 3, reference 315 and 370, col. 12, lines 35-42).

For claim 7, Herring discloses wherein the memory system further comprises at least one of a random access memory, a synchronous dynamic random access memory, a synchronous dynamic random access memory controller, a static random access memory controller, and a nonvolatile memory (figure 4, references 410, 420, 430 and 440, col. 15, lines 36-45).

For claim 8, Herring discloses wherein the memory system further comprises a memory bus, wherein the memory bus is adapted to couple one or more bus interfaces to one or more memory controllers (figure 4, references 410, 420, 430 and 440, col. 15, lines 36-45).

For claim 24, Herring discloses packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path, comprising:

receiving means to receive a network packet at a first port (figure 3, reference 310) (col. 12, lines 11-12);

transmitting means for transmitting the network packet after processing, the

receiving means in communication with the transmitting means (col. 12, line 24);

means for associating a first control information with a first portion of the network packet (col. 9, lines 30-39);

means for associating second control information with a second portion of the network packet (col. 9, lines 30-39);

means for processing the first portion of the network packet and the second portion of the network packet at least partially in parallel (col. 9, lines 30-39); and

means for enqueueing the first portion and the second portion for transmitting to a second port in the same order in which the first portion and the second portion were received at the first port (col. 12, lines 35-38).

For claim 25, Herring discloses wherein the means for processing the first portion of the network packet and the second portion of the network packet at least partially in parallel is implemented at least partially in software (col. 9, lines 30-34).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3, 5 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herring (US 6,606,326) in view of Rosborough et al. (US 6,493,754).

For claims 3, 5 and 9, Herring disclose wherein the processor comprises one or more microengines (figure 1, reference 15, col. 9, lines 31-34) to execute program threads, the threads include receive schedule program threads to assign the first portion of the network packet from the first port to a first receive processing program thread and the second portion of the network packet to a second receive processing program thread, wherein the bus interface is responsive to the one or more microengines, and wherein the first and second receive processing program threads are adapted for processing and enqueueing (figure 3, reference 350)(col. 12, lines 35-38).

For claim 9, Herring disclose wherein the processor comprises one or more microengines (figure 1, reference 15) to execute program, wherein the one or more microengines are configured to operate with shared resources, and wherein the shared resources comprise the memory system (figure 4, references 350 and 410-440) and the one or more peripheral buses (figure 3, reference 315 and 370)(col. 9, lines 30-34).

However, Herring does not expressly disclose program threads. In an analogous art, Rosborough et al. disclose program threads (col. 6, line 39).

Rosborough et al. disclose wherein the bus interface uses sequence numbers to enqueue the first portion and the second portion, wherein the bus interface is to associate one or more first portion sequence numbers with the first portion and one or more second portion sequence numbers with the second portion as the first and second portions are received from the first port (col. 9, lines 35-42 as set forth in claim 4); wherein the bus interface is further to maintain a second set of sequence numbers for use by the first and second receive processing program threads in determining the order in which the first and second portions are to be enqueued (col. 9, lines 35-42 as set forth in claim 5);

One skilled in the art would have recognized the program threads, and would have applied Rosborough et al.'s threads in Herring's processing element 15. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Rosborough et al.'s method and apparatus for analyzing communications on different threads in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being identified such that it can have only one service request on it at a given point in time (col. 6, lines 44-48).

For claim 10, Herring disclose wherein the bus interface comprises an input-output bus interface (figure 3, reference 315 and 370, col. 12, lines 35-42).

For claim 11, Herring disclose wherein the bus interface is coupled to an input-output bus, wherein the input-output bus is coupled to a dual gigabit MAC (figure 3, reference 315 and 370, col. 12, lines 35-42).

For claim 12, Herring disclose wherein at least one of the microengines comprises:

a control store for storing a microprogram; and a set of control logic, wherein the set of control logic comprises an instruction decoder and one or more program counter units (col. 14, lines 13-18).

For claim 13, Herring disclose wherein at least one of the microengines further comprises a set of context event switching logic to receive messages from the shared resources (col. 14, lines 13-18).

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herring (US 6,606,326) in view of Boucher et al. (US 6,226,680).

For claim 14, Herring discloses packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path, comprising:

controller (figure 3, reference 340) comprising one or more ports (figure 3, references 310 and 380, col. 11, lines 62-65).

However, Herring does not expressly disclose:

a media access controller capable of providing one or more status flags;

a bus interface unit comprising one or more registers, wherein the one or more registers comprise control registers and status registers;

a bus connected between the media access controller and the bus interface unit; and a sequencer to poll the one or more status flags and place the one or more status flags to the one or more registers over the bus, wherein the communication system is capable of processing one or more packets of data, and wherein the communication

system is capable of maintaining an intra-packet order and an inter-packet order for the one or more ports. In an analogous art, Boucher et al. disclose:

a media access controller (figure 13, references 210) capable of providing one or more status flags (col. 18, lines 27-29);

a bus interface unit (figure 13, reference 468) comprising one or more registers (figure 14, references 490, 496 and 501), wherein the one or more registers comprise control registers and status registers (col. 16, lines 64-65);

a bus connected between the media access controller (figure 13, references 210) and the bus interface unit (figure 13, reference 468); and

a sequencer (figure 7, reference 176) to poll the one or more status flags and place the one or more status flags to the one or more registers over the bus, wherein the communication system is capable of processing one or more packets of data, and wherein the communication system is capable of maintaining an intra-packet order and an inter-packet order for the one or more ports (col. 9, line 66 to col. 10, line 4).

One skilled in the art would have recognized the media access controller, and would have applied Boucher et al.'s media access controller 172 in Herring's processing system 5. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Boucher et al.'s intelligent network interface system method for protocol processing in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being received message packet (col. 9, line 55).

9. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herring (US 6,606,326) in view of Rosborough et al. (US 6,493,754) further in view of Boucher et al. (US 6,226,680).

For claims 15 and 17-19, Herring in view of Rosborough et al. does not expressly disclose wherein the media access controller further comprises one or more transmit registers and one or more receive registers, and wherein the one or more ports comprise at least two gigabit Ethernet ports. In an analogous art, Boucher et al. disclose wherein the media access controller further comprises one or more transmit registers and one or more receive registers, and wherein the one or more ports comprise at least two gigabit Ethernet ports (col. 16, lines 64-65).

Boucher et al. disclose wherein the one or more status flags comprise one or more transmit status flags and one or more receive status flags, and wherein the one or more flags indicate whether an amount of data in associated transmit registers and associated received registers have reached a threshold level (col. 18, lines 27-29 as set forth in claim 17); wherein a receive scheduler thread uses the one or more registers in the bus interface unit to determine how to issue a receive request (col. 17, lines 7-12 as set forth in claim 18); and wherein the communication system uses a set of sequence numbers for each port, wherein the sequence numbers comprise a network packet sequence number, a MAC packet sequence number, and an enqueue sequence number (col. 10, lines 27-35 as set forth in claim 19).

One skilled in the art would have recognized the media access controller, and would have applied Boucher et al.'s media access controller 172 in Herring's processing

system 5. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Boucher et al.'s intelligent network interface system method for protocol processing in Herring's packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path with the motivation being received message packet (col. 9, line 55).

For claim 16, Herring discloses wherein the communication system is capable of enqueuing a first portion of a network packet and a second portion of a network packet for transmission to a second port in the same order in which the first portion and the second portion were received at a first port (col. 12, lines 35-38).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOAN D. NGUYEN whose telephone number is (571)272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on 571-272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. D. N./
Examiner, Art Unit 2416

/FIRMIN BACKER/
Supervisory Patent Examiner, Art Unit 2416